PATENT
Customer No. 22,852
Attorney Docket No. 04329.2270-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re 53(b) Continuation Application of:	)	
	)	
Shinsuke SAKAMOTO et al.	)	Group Art Unit: 2815
	)	
Application No.: 09/527,563	)	Examiner: E. Lee
	)	
Filed: March 16, 2000	)	
	)	
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND WIRING ARRANGING METHOD THEREOF	)	

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the examination of the above application, please amend this application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 1, replace the paragraph beginning on line 11 with the following:

The present invention relates to a semiconductor integrated circuit device making use of an area pad and a wiring arranging method thereof.

On page 9, replace the paragraph beginning on line 22 with the following:

As described above, the wiring length of the I/O slot can be shortened by the rewiring 24, 33 on the outermost periphery of the chip, and the delay in the signal

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

transmission can be improved by the shortening of the I/O slot wiring. The improvement of the delay in the signal transmission will now be described.

On page 12, replace the paragraph beginning on line 2 with the following:

Incidentally, the I/O slot to be replaced is not limited to the adjacent slot. For example, the rewiring 24, 33 as shown in FIG. 1 can be extended to reach the wiring in the outermost peripheral area such as the I/O slots 11c and 11d. It is also possible to interchange the I/O slots apart from each other by at least two slots.

IN THE CLAIMS:

Please cancel claims 2 and 3 without prejudice or disclaimer of the subject matter thereof, amend claim 1, and add new claims 4-14, as follows:

1. (Amended) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged above said first I/O slot;

a second pad arranged above the first I/O slot and a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward a central portion;

a first wiring having one end positioned in said first pad and having the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring having one end positioned in the second pad and having the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

a third wiring arranged in an outermost peripheral portion of the chip and serving to connect the other end of the first wiring to the second I/O slot, the third wiring being isolated from the second wiring; and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being isolated from the first wiring.

Please add the following new claims:

4. (New) The semiconductor integrated circuit device according to claim 1, wherein the third wiring and the fourth wiring do not overlap.

5. (New) The semiconductor integrated circuit device according to claim 1, wherein the fourth wiring is shorter than the third wiring.

6. (New) The semiconductor integrated circuit device according to claim 1, wherein the first and second I/O slots, the first and second pads and the first wiring and the second wiring are each designed and fixed in advance.

7. (New) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are the same in wiring level.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

8. (New) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

9. (New) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged above the first I/O slot:

a second pad arranged above the first I/O slot and a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward a central portion;

a first wiring having one end positioned in the first pad and having the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring having one end positioned in said second pad and having the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to the second I/O slot; and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being shorter than the third wiring.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

10. (New) The semiconductor integrated circuit device according to claim 7, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

11. (New) The semiconductor integrated circuit device according to claim 7, wherein the third wiring and the fourth wiring do not overlap.

12. (New) The semiconductor integrated circuit device according to claim 7, wherein the first and second I/O slots, the first and second pads and the first and second wiring are each designed and fixed in advance.

13. (New) The semiconductor integrated circuit device according to claim 7, wherein the first wiring and the second wiring are the same in wiring level.

14. (New) The semiconductor integrated circuit device according to claim 7, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

IN THE DRAWINGS:

Subject to the approval of the Examiner, please amend Fig. 4 by including the legend "Prior Art", as proposed in the accompanying "Request for Approval of Drawing Change" filed herewith.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

REMARKS

By this Preliminary Amendment, Applicants cancel claims 2 and 3 without prejudice or disclaimer of the subject matter thereof, amend claim 1, and add new claims 4-14. Thus, the pending claims are claims 1 and 4-14.

CONCLUSION

Attached hereto is a marked-up version of the changes made to the claims and specification by this amendment. The attachment is captioned "**Appendix to the Preliminary Amendment of February 25, 2002**" Deletions appear as normal text surrounded by [ ] and additions appear as underlined text.

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 25, 2002

By: Tara Bleech
Tara L. Bleech
Reg. No. 46,559

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Application Number: To be assigned
Filing Date: February 25, 2002
53(b) Continuation application of:
Application Number: 09/527,563
Filing Date: March 16, 2000
Attorney Docket Number: 04329.2270-01

APPENDIX TO PRELIMINARY AMENDMENT OF FEBRUARY 25, 2002

Amendments to the Specification

Please amend the specification as follows:

On page 1, replace the paragraph beginning on line 11 with the following:

The present invention relates to a semiconductor integrated circuit device [make] making use of an area pad and a wiring arranging method thereof.

On page 9, replace the paragraph beginning on line 22 with the following:

As described above, the wiring length of the I/O slot can be shortened by the rewiring 24, [23] 33 on the outermost periphery of the chip, and the delay in the signal transmission can be improved by the shortening of the I/O slot wiring. The improvement of the delay in the signal transmission will now be described.

On page 12, replace the paragraph beginning on line 2 with the following:

Incidentally, the I/O slot to be replaced is not limited to the adjacent slot. For example, the rewiring 24, [23] 33 as shown in FIG. 1 can be extended to reach the wiring in the outermost peripheral area such as the I/O slots 11c and 11d. It is also possible to interchange the I/O slots apart from each other by at least two slots.

Amendments to the Claims

Please amend claim 1, as follows:

1. (Amended) A semiconductor integrated circuit device, comprising:

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

[a plurality of] first and second I/O slots arranged in parallel along [the] a peripheral portion of a chip within [the] an inner region of the chip and [having] connected to input/output cells [connected thereto] of the chip;

a [plurality of pads] first pad arranged [a predetermined distance apart from each other] above said first I/O slot [and extending from the peripheral portion of the chip toward the central portion];

a second pad arranged above the first I/O slot and a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward a central portion;

a [plurality of] first wiring [each] having one end positioned in said first pad and having the other end positioned in the peripheral [region] portion of the inner [portion] region of the chip above the first I/O slot; [and]

a second wiring having one end positioned in the second pad and having the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a [second] third wiring arranged in [the] an outermost peripheral [region] portion of the chip and serving to connect the other end of [each of the plural] the first wiring to [a predetermined] the second I/O slot, the third wiring being isolated from the second wiring; and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being isolated from the first wiring.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

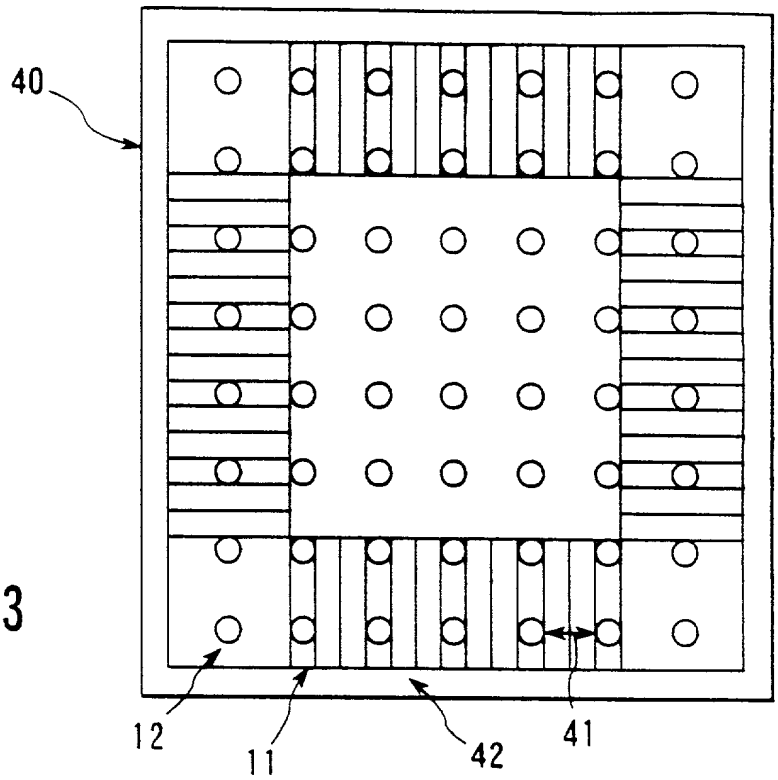

FIG. 3

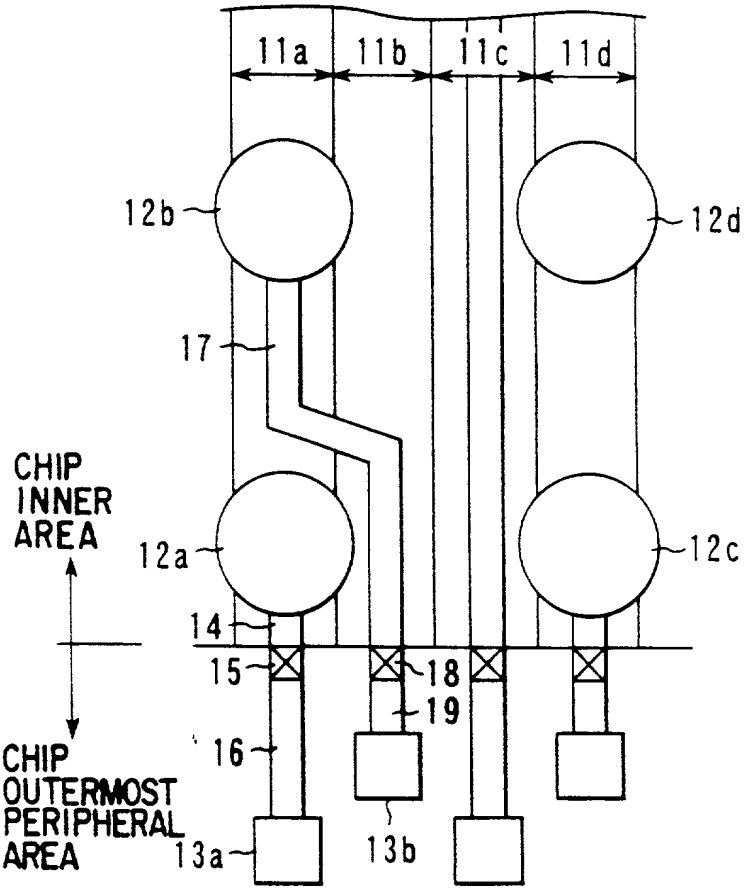

FIG. 4

Prior Art